...We *are* boundary-scan.

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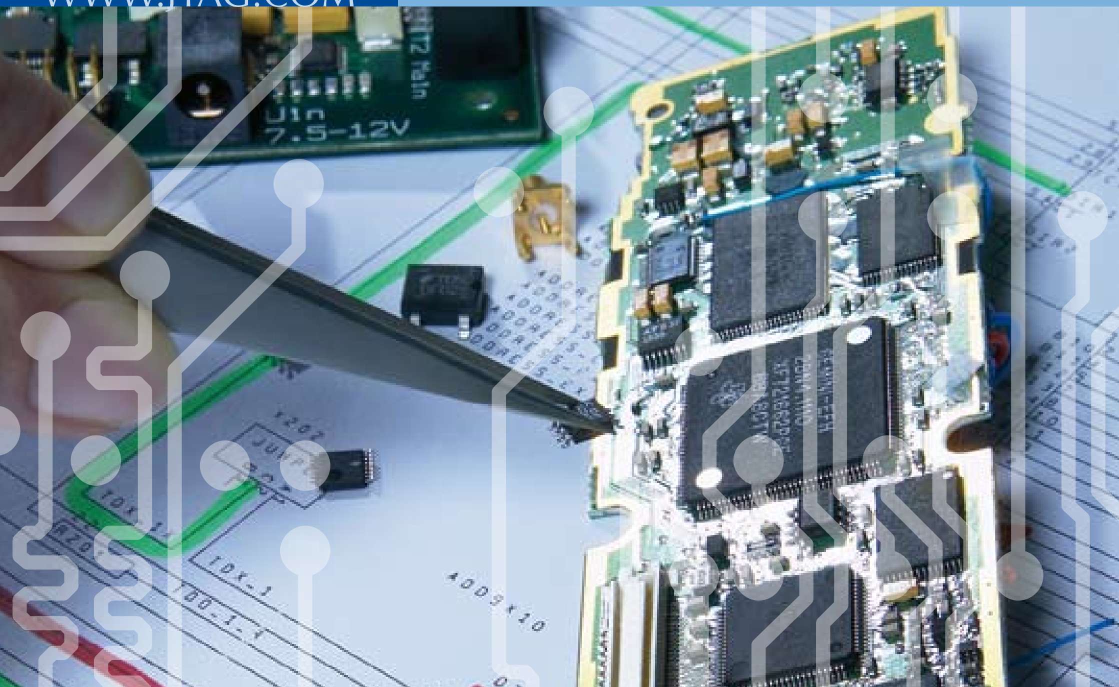

Board DFT Guidelines

...We *are* boundary-scan.

This booklet has been prepared with great care, but yet might contain inconsistencies. The reader is welcome to give any comment or suggestions.
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Design for Test Guidelines For Board Testing and In-System Configuration

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Preface:

Boundary-Scan Technology
For PCB Testing and In-System Configuration

Why boundary-scan?
Throughout the electronics industry, manufacturers are turning to the latest device technologies, such as ballgrid arrays (BGAs), chip-scale packages, and other small outlines, to provide the functionality and miniaturization they need. However, the new packages are increasing the difficulty of accessing printed circuit boards for In-Circuit Testing (ICT) and in-system device configuration. These difficult access problems have been addressed by the industry through adoption of the IEEE 1149.1 boundary-scan standard, allowing pin-level access - independent of the device packaging technology - to even the most crowded assemblies. Nowadays almost all popular complex ICs are supporting IEEE Std 1149.1 test features. On printed circuit board level it is the responsibility of the hardware designer to use the available IC IEEE 1149.1 features for achieving a better board level testability. The guidelines described in this booklet help the designer to implement board level DFT.

Benefits of boundary-scan
The result is a reduction in the number of test points needed on the board giving simpler board layouts, less costly test fixtures, reduced time on the in-circuit tester, and faster time-to-market. On the programming side, boundary-scan allows configuring almost all types of CPLDs and flash memories, regardless of size or package type, on the board, after PCB assembly.

You'll realize substantial savings by reducing device handling, decreasing the burden of inventories of pre-programmed parts, and integrating the programming steps into the board production line.

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1 Introduction

So, at last you've managed to grab a five minute break to take a closer look at what you can do with that puzzling interface people have been talking about - the JTAG port. If you've studied it in detail you will have realised that by using the completely autonomous JTAG port you can access all the pins (except analogue, power and grounds) of a JTAG compliant part with the core logical function effectively disconnected or suspended. This means that via a minimal 4 wire bus you can use test patterns (vectors) to toggle signals at output or I/O pins and monitor inputs at sense or I/O pins to establish whether or not interconnects (nets) are as per your design.

If you are a design engineer reading this then you will already have acknowledged the role you must play in DFT (Design for Test). If however you are a test or production engineer it is vital that you establish contact with designers at the earliest planning stages of a new design and gain their co-operation to implement some of the ideas mentioned below. In either instance it is clearly advantageous to have regular meetings on a products test strategy (for prototype debug, production and field service) as soon as product concepts are known.

The scope of this document is to present a number of Design-for-Test guidelines that can be used for reference in support of implementing boundary-scan architecture within PCB designs. So that the test fraternity can utilise this architecture effectively in performing board level manufacturing structural testing and the in-system configuration of cPLD, FPGA's and flash memory devices.

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2 Considerations for Implementing Board Level Boundary-Scan

2.1 Component Selection

2.1.1 Select IEEE Std. 1149.1 Compliant Devices

The first thing to be considered in implementing boundary-scan test architecture within any PCB design is careful component selection. Ensure that 1149.1 compliant components are selected where possible. It is normally the case that modern day VLSI devices are 1149.1 compliant, however, it is often the case that with small scale integrated devices there will be a choice between selecting compliant or noncompliant parts from differing silicon providers that perform the same core function. If possible select the 1149.1 compliant device as this will increase your boundary-scan test coverage.

2.1.2 Dual Function JTAG Port Pins

Try and avoid the selection of devices that assign dual functionality to the JTAG port pins. This is often the case where the silicon provider has decided that it is not cost effective to add a minimum of four additional boundary-scan access pins, purely for test purposes. In this instance they have chosen to multiplex the JTAG control signals with pre-defined core function signal pins.
In these circumstances the device dual function pins will default to core function mode on power-up, and will have to be forced into the JTAG mode of operation by selecting the appropriate drive state on a pre-defined JTAG Enable pin. Once boundary-scan tests have been completed the JTAG enable pin can revert to its non-active state.
Where possible try and avoid the selection of devices that multiplex the boundary-scan control pins with device core function pins, as this will often require the multiplexing of the dual function signal lines external to the device via glue logic and will require additional access to a JTAG ENABLE pin in order to place the device in boundary-scan mode.
Note: - It is not always possible to select an alternative device that is fully 1149.1 compliant. In the situation where there are no alternative choice, designers must ensure that the JTAG ENABLE can be accessed prior to executing board level boundary-scan tests.

2.1.3 Check BSDL Files for Non-Compliance of 1149.1 Std.

Ensure that the data sheets and bsdl files are thoroughly checked for information specifying noncompliance to the IEEE 1149.1 Std. This is often specified in the bsdl file as a design attribute or a compliance patterns attribute as detailed below.

```
attribute DESIGN_WARNING of SA1110: entity is                   -- (ref B.8.18)
" 1.IEEE 1149.1 circuits on SA1110 are designed                          " &
" primarily to support testing in off-line module                        " &
" manufacturing environment. The SAMPLE/PRELOAD                          " &
" instruction support is designed primarily for                          " &
" supporting interconnection verification test and not                   " &
" for at-speed samples of pin data.                                      " &
" 2.Ensure to drive BATTF and VDDF to logic level 0 else the chip        " &
" will sleep!                                                             ";
```

In the above example for the Intel StrongArm processor, the attribute DESIGN WARNING specifies that the BATTF and VDDF signal pins must be driven to a logic "0" state; otherwise the chip will go into the sleep mode.

```
Attribute COMPLIANCE_PATTERNS of XC2S150_FG456 : entity is "(PROGRAM) (1)";
```


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In this example for the Xilinx SPARTAN XC2S150 fpga; the attribute COMPLIANCE PATTERNS specifies that the device PROGRAM pin must be driven to the logic “1” state for the device to function in boundary-scan mode.

2.1.4 Supported Instructions

All IEEE Std. 1149.1 compliant devices must support the mandatory SAMPLE/PRELOAD, EXTEST and BYPASS instructions. However, it is highly desirable if devices also support the optional instructions of HIGHZ and IDCODE. The IDCODE instruction is particularly useful for determining whether the correct device has been placed during the manufacturing process by reading the 32-bit device IDENT register which will specify the manufacturer’s details, the device type code provided via the JEDEC committee and a 4-bit revision code.

The revision code is particularly useful in situations where there are multiple versions of devices that have the same package footprint, but the internal functionality differs. In this situation it is more cost effective to detect the revision status at the process verification test stage, instead of the functional or system test stages.

The HIGHZ instruction is extremely useful for optimising the length of boundary-scan chains, particularly when programming flash memory on a target board. It is imperative that the overall boundary-scan data register is kept to a minimum number of cells required for accessing the target flash memory data, address and control lines.

If multiple boundary-scan devices are accessing the address and data bus connected to the target flash, these signal pins will have to be held in a high impedance state during memory read/write cycles in order to avoid bus contention.

If these contending devices support the HIGHZ instruction, it will only require a few bits (>2) to provide the instruction to place the contending output pins in a high impedance state. However, if contending devices do not support the HIGHZ instruction, the safe state value will have to be shifted into the control cells of all the contending output signal pins. This could mean a substantial increase in the number of bits that require shifting for each flash memory read/write cycle.

2.1.5 IEEE Std. 1532 Support

It may be advisable to select cPLD devices that are compliant with the IEEE 1532 Std. for in-system configuration, as this will allow multiple cPLD devices from different silicon vendors to be configured simultaneously. However, if it is not possible to select 1532 compliant devices, these devices can still be configured in isolation by programming one device at a time.

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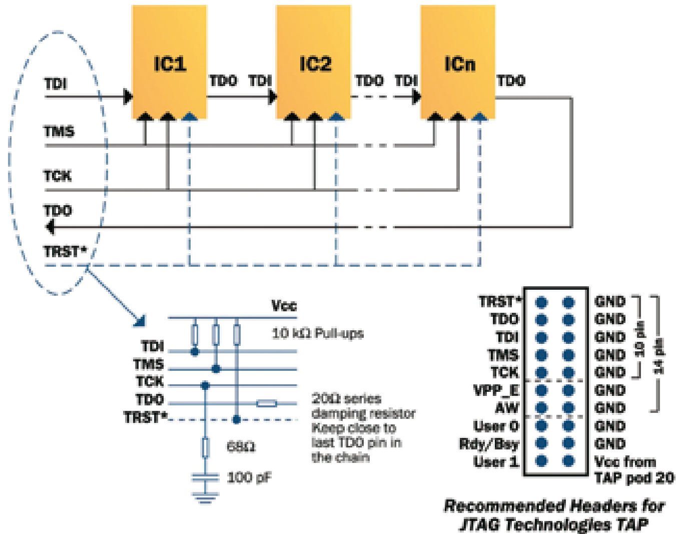
2.2 Scan Chain Layout - Design Partitioning

2.2.1 Connection of JTAG Control Signals

Ensure that all the JTAG test access port (TAP) control signals; TCK, TMS and optional TRST are connected in parallel. TDI and TDO are used to "daisy chain" boundary-scan devices into a chain path as detailed in Figure. 1

Figure. 1 - JTAG Signal Terminations



Note:- In some circumstances it may be necessary to construct more than one chain. For example:

2.2.2 Partitioning - Third Party Debugging/Emulation Tools

When devices must be kept in a separate chain in order to be compliant with third-party debugger or emulation tools. An example of this is an IC vendors DSP debugging software tool which expected every device in the chain to have an instruction register length of 4-bits.
This of course cannot be guaranteed, subsequently in this instance all the DSP devices would be layed out in a separate chain.

2.2.3 Partitioning - Different FPGA and cPLD Vendors

It may be necessary to place FPGA and cPLD devices from particular silicon vendors in separate chains so that the associated proprietary in-system configuaration tools i.e. Xilinx's; JTAG Programmer, Altera's; ByteBlaster and Lattice Semiconductor's; ispDownload software can communicate with their devices.

Note:- This does not become a problem if the in-system configuration devices are IEEE 1532 Std. compliant, because all devices will comply with this standard and subsequently can be configured simultaneously in any device combination.

2.2.4 Partitioning - Different Logic and Voltage Families

It may be advantageous to segment different logic families e.g. ECL / TTL or voltage families e.g. 1.8V, 2.5V and 3.3V by placing the different families of devices into separate chains.
Connect the external TAP connections to the individual chains and ensure that the external controller can select the appropriate drive levels.

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Alternatively group the voltage families so that all the 3.3V devices are daisy-chained together. These will then daisy-chain into the next voltage family group i.e. 1.8V, but the boundary-scan control signals and TDO signal from the last device in the 3.3V group will have to go through a voltage converter to reduce the voltage to 1.8V.

2.2.5 Partitioning - Optimised Test Vector Execution

It may also be advantageous to segment devices into separate chains for improved test partitioning and diagnostic resolution, or for optimising the test vector execution.
This is particularly important for flash memory programming, where care must be taken to optimise the overall boundary-scan register length so that the minimal number of boundary-scan register (BSR) bits are shifted for each flash memory read/write operation. In may be advisable to segment a particular functional block of boundary-scan devices into a separate chain, so that only the device accessing the address, data and control signals of the target flash memory is operating in EXTEST mode, with the other devices in the chain configured for BYPASS or HIGHZ.

2.2.6 Partitioning - Board-to-board Interconnect Testing

It is also advantageous in system level applications to partition devices that provide access to the backplane interface to be segmented into a separate boundary-scan chain. This will optimise the test vector execution for board-to-board interconnect testing between multidrop boards configured within a sytem level environment.

2.2.7 Signal Termination

For high-speed (vector intensive) JTAG applications such as SDRAM testing, or Flash Programming configurations where TCK speed of >10MHz are used, it is advisable to terminate the TCK line using an impedance matched RC network comprising a resistor (close to the characteristic impedance of the TAP cable, e.g. 60-100 Ohms and capacitor e.g. 100pF) in series to ground. All other JTAG inputs should be pulled high using a weak (10Kohm) pull-up resistor. To damp reflections a 22 Ohm series resistor can also be implemented between the last device in a chain and the UUT TDO pin.

2.2.8 Edge Connector Access

Where possible access to the boundary-scan chain / chains should be via the edge connector, as this will eliminate the need for bed-of-nails probing of test points or test vias which can often lead to unreliable testing due to poor pin contact resulting from no-clean manufacturing processes. This would also be preferable for system level access within a backplane environment.

2.2.9 Power Distribution

On boards comprising of hybrid analog/digital design it may be dangerous to drive boundary-scan patterns on the digital portion of the circuit causing random behaviour from the analog portion. For example if the analog circuit was providing some power handling capability, this could lead to the potential damage of devices or to the board. This can be alleviated by designing analog and digital subsystems that allow the analog power to be shut-down whilst boundary-scan tests are executed.

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2.3 Scan Chain Layout - Signal Integrity

2.3.1 Tracking of TCK and TMS

It is imperative that the tracking of the TCK and TMS signals are kept as short possible, thus eliminating any trace looping. Specify the routing of these signals within the PCB layout auto route tools as CRITICAL.

2.3.2 Buffering and Fan-out of JTAG Signals

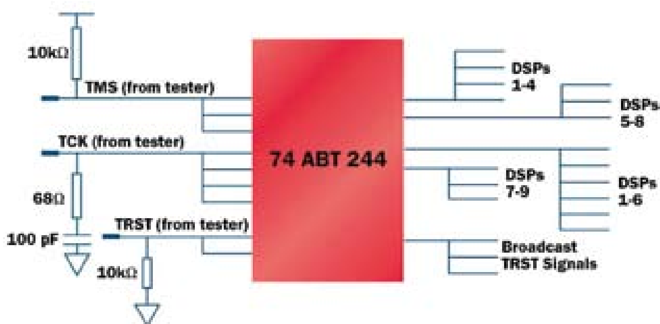
It is good practice to buffer all the IEEE Std. 1149.1 input signals interfacing to the board to ensure good signal integrity, in particular TCK and TMS.

Once on the board, fan-out of the control lines (TMS, TCK) may also have to be considered. A general rule of thumb is that if track lengths are relatively short, then fan-out to 4 - 6 devices from a 74244 type buffer is acceptable. However, if track lengths between the buffer device and boundary-scan devices are fairly long (> 10 cms), a fan-out to 1 - 2 devices would be advisable. Refer to Figure.2

It is worthwhile considering buffering the primary asynchronous reset signal (TRST) and terminating this signal with a weak pull-down resistor (typically around 10K ohm) that can be easily driven by a PC based boundary-scan controller. The buffer ensures that the broadcast secondary TRST signal can overcome the parallel sum of internal device pull-up resistors.
If the buffer was not present, the weak pull-down would have to contend with the parallel sum of the internal pull-up resistors, which would prevent an asynchronous reset from occurring once external control of the primary TRST line was relinquished.

The pull-down termination is preferred by the majority of designers because once the externally connected scan-controller relinquishes control, the primary TRST signal will be pulled low by the onboard pull-down, driving all the secondary TRST lines low and forcing the down stream boundary-scan devices into Test-Logic-Reset (TLR), returning the board to its operational state.
Note: - The above signal integrity considerations may be considered as over cautious, but it may be the difference between devices functioning reliably or not at all.

Figure. 2 - Fan-out of TCK and TMS



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2.4 Scan Chain Layout - Physical Bypassing

2.4.1 Physical Bypassing

It may be pertinent to place zero ohm bypass resistors so that via a combination of DNP (do NOT place) and placed resistors boundary-scan devices can be pysically bypassed within a boundary scan chain as shown in Figure.3.

This implementation is certainly advisable during prototype builds where it is quite possible that although silicon provided by the IC vendor has the additional boundary scan pins within the device package to allow access to the boundary scan functionality. It is often the case, that due to time to market pressures, the boundary scan silicon has either not been implemented or has not been tested, in which case it will not function as expected. If these devices form part of the on-board boundary scan infrastructure, you will now have an incomplete chain and subsequently will not be able to test any of the board using boundary scan.

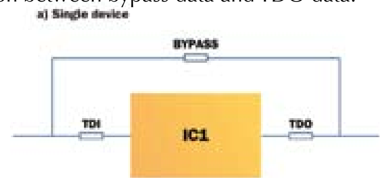
2.4.2 Single Device Bypass

In configuration (a) the zero ohm series resistors connected to the TDI and TDO pins will normally be fitted and the BYPASS resistor will be a DNP. However, if this device needs to be bypassed in order to get the chain to function, the BYPASS resistor will be placed and the TDI and TDO resistors removed.

The TDI resistor is removed to prevent erroneous instructions from being shifted into the bypassed device instruction register (remember that the TCK and TMS signals will still be connected, subsequently the device TAP controller will still be active). The IEEE 1149.1 Std, specifies that all compliant devices should have an internal pull-up on the TDI pin, which will ensure that an all 1's instruction will be shifted into the bypassed device instruction register - the all 1's value is the BYPASS instruction.

The TDO resistor is removed to prevent signal contention between bypass data and TDO data.

Figure. 3 - Physical Bypass of Sin gle and Multiple Devices

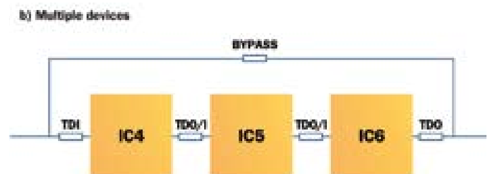


2.4.3 Multiple Device Bypass

Configuration (b) shows the bypassing of multiple devices, which may be a group of memory devices that are beta release silicon. In this instance it is advisable that the facility to bypass all these devices is implemented within the board design.

The only difference between this implementation and the single device implementation, are the additional TDO/TDI zero resistors between each device within the bypass group. This is to ensure that by removing these resistors the Capture-IR instruction values will not be shifted into the downstream device, which may cause erroneous operation of the device causing the device IO pins to be driven to an unknown state.

Note: - These configurations should only be necessary for prototype designs that utilise virgin silicon, as it should be anticipated that any silicon problems are resolved prior to commencing full production.



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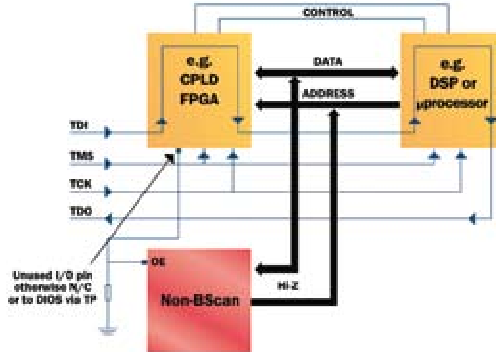
2.5 Control of Non- Boundary Scan Devices

2.5.1 Access to Control Signals of Non-Scan Logic

It is imperative that the control signals of non-boundary scan devices are connected to boundary-scan cells, so that these devices can be disabled during test in order to prevent any signal contention which could cause damage to devices or cause the tests to be unreliable.

Figure. 4 - Control of Non-Boundary Scan Devices



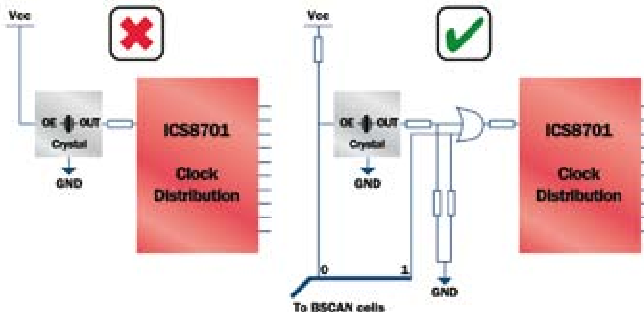
In the above example (Fig.4) the non-boundary scan device is also accessing the data and address busses that are being tested as part of the interconnect test between the two boundary scan devices. In this instance the OE control pin of the non-boundary scan device, must be connected to a boundary scan cell so that it can driven to a logic “1” state to disable this device during interconnect testing, so that it’s output pins are placed in a high impedance state and will not impede testing of the data and address busses.

In the example above the OE pin of the non-boundary scan device is connected to an unused pin of aboundary scan device (in this instance an fpga device) which is not connected internally to any mission mode logic. This signal is not driven during normal operation (it is held low via the pull-down resistor), but for test purposes it is controlled via a boundary scan cell.

2.5.2 Control of Clock Signals

It may also be necessary to gain control of clock signal pins that are utilised to synchronize the memory read/write access to SSRAM and SDRAM devices. Subsequently it is imperative that the on-board clock can be disabled and replaced with a test clock as detailed in Figure. 5.

Figure. 5 - Control of Clock Signals



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The clock distribution circuit in the left hand side example is an indication of how not to implement clock distribution. In this instance the on-board oscillator cannot be disabled because its OE control line is tied directly to VCC, and there is no facility for boundary-scan access to the primary clock distribution signal.

However, the implementation in the right hand side example has accommodated the disabling of the on-board oscillator by connecting the OE pin to a spare boundary-scan cell (this could be an unused IO pin on an fpga or cPLD, that is not connected to internal core logic) and driving this signal pin to a logic "0" to place the OUT pin of the on-board oscillator in the high impedance state. This will allow the on-board clock to be replaced by a test clock which is driven from a spare boundaryscan cell functioning in EXTEST mode via the gating circuitry shown. The test clock will be distributed to all the devices controlled via the clock distribution device including SSRAM and SDRAM memory devices. Note that in some circumstances this could equate to potentially 20% - 30% of the boundaryscan test coverage within the board design.

Note: - When using this technique, check on the minimum operating frequency of the clock distribution device as this may require a minimum operating frequency to synchronise with the internal PLL.

2.6 Special Considerations for SRAM based FPGA Devices

2.6.1 Boundary Scan Execution - Pre and Post Configuration

SRAM based FPGA devices are often subject to changes to their boundary scan behaviour at different stages during the programming / configuration cycle. During the power-up cycle these devices will enter a configuration phase which will prevent the boundary scan circuitry from being accessed, unless the configuration sequence can be held-off.

Note: - Carefully read the manufacturer's data sheets / application notes to determine whether this may be a problem. In particular any reference to a **compliance pattern** *attribute within the bsdl file i.e.* ***"(INIT,PROGRAM) (01)"****; This specifies that INIT and PROGRAM pins should be held in the logic '0' and logic '1' states respectively to place the device in boundary-scan mode.*

2.6.2 Xilinx XC4K and Spartan Considerations

In the case of the Xilinx XC4K and early Spartan devices, the PROG pin needs to be held high to enable EXTEST operations whilst the INIT pin tied needed to be tied low so that during power-up these devices are prevented from entering the configuration cycle. This can be achieved by placing headers on the board so that jumpers can be placed to ensure the appropriate pin status on power-up. During normal operation, once the devices have configured, the boundary scan mode of operation will be available which will enable boundary scan tests to be conducted. Refer Figure.6a.

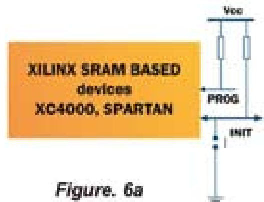

Figure. 6a

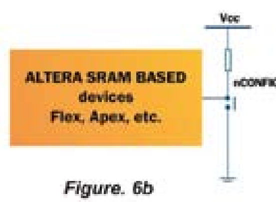

Figure. 6b

2.6.3 Altera FLEX and APEX Considerations

In the case of the Altera FLEX and APEX family of devices carefully read the documentation, because there are some instances particularly with the FLEX 6000 devices where the default condition is that the JTAG functionality is disabled, unless this feature is enabled during device bit stream generation. However, even if this feature is enabled it is still not possible to execute boundary scan tests during preconfiguration unless the nCONFIG signal line is held low (Figure 6b) in order to hold the device in reset, whilst a low to high transition will start the configuration phase. Configuration can be prevented by connecting the nCONFIG signal line via a jumper to GND.

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The alternative to executing tests pre-configuration is to wait until the FPGA has configured, at which time JTAG functionality will be available. However, it may be necessary to obtain a BSDL file that describes the post-configuration status as some of the IO pins may now be re-defined following configuration. Refer to section 2.7.

2.6.4 Xilinx Spartan 2/3 and Virtex Considerations

Figure. 6c

In the case of the Xilinx Spartan 2 and 3 series and the Virtex family of devices a logic '0' on the PROGRAM pin resets the TAP controller and no boundary-scan tests are possible. This is clearly defines as a compliance pattern attribute in the bsdl file, stipulating that this pin should be pulled-high. It is also important not to develop boundary-scan tests that toggle the PWRDWN pin as this will cause the device to enter power-down mode, in which case the boundary-scan function will no longer be available. Refer to Figure 6c.

2.7 FPGA Re-configurable I/O Considerations

2.7.1 Pre and Post Configuration BSDL Files

All the I/O pins of FPGA devices are defined as bi-directional in the pre-configured state, which means that each of the IO pins is connected to three boundary-scan cells as defined in Figure.7a; input cell, output cell and control cell.

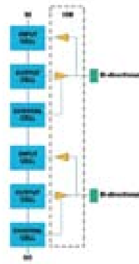

Figure. 7a - Pre-configuration

Figure. 7b Post-configuration (LVDS - Rx)

A number of the FPGA devices available from the silicon vendors now allow reconfiguration of the IO blocks (IOB's) to support a wide variety of I/O standards. However, the selectable I/O resource can change the function of the boundary-scan cell architecture behind the reconfigurable IOB. The example in Figure.7b for a LVDS input receiver configuration shows how the boundary-scan cell status has changed to that of a single input cell, with the remaining five cells having no boundary-scan function other than that of internal cells to complete the chain.
This means that boundary-scan tests developed for the pre-configured state cannot be used once the device has been configured. In this case tests will need to be regenerated that comply with the postconfiguration boundary-scan status as described in a post-configuration bsdl file.

Note: The FPGA tool vendors provide a utility to automatically create a post-configuration bsdl file post-configuration interconnect testing. Xilinx provide a BSDLAnno utility (refer to # 15346) in the Xilinx Knowledge Database that obtains the necessary design information from the "ncd" file for FPGA's and the "pnx" file for cPLD's and generates a bsdl file that reflects the post-configuration boundary-scan architecture.

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2.8 Flash Programming Optimisation

2.8.1 AutoWriteTM Access

The importance of optimizing the flash programming sequence was discussed earlier in sub-paragraph 2.2.2.6 which emphasized the need to keep the chain length to an absolute minimum. This process can be enhanced further by utilizing JTAG Technologies AutoWriteTM feature which utilises a WE strobe pulse for each flash memory write cycle access, instead of accessing each address three times in order to toggle the WE signal. As shown in Figure.8 this is achieved by routing the WE signal to the edge connector (or to a header if this is feasible) so that it can be connected to the AW (pin 13) pin on the JTAG Technologies TAP pod.

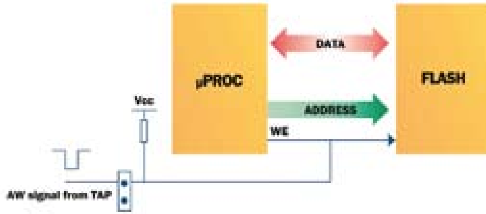

Figure. 8 - AutoWriteTM Access

2.8.2 Eliminating Signal Contention

In order to utilise this facility it is essential that the boundary scan cell that is driving the WE signal (in this example from the processor) can be placed in the high impedance state, otherwise there will be contention between the processor WE signal and the AW signal generated via the TAP pod.

Figure.9 below shows how this is controlled via the control cell associated with the output cell driving the WE signal, and how this is represented within the BSDL file boundary scan register description.

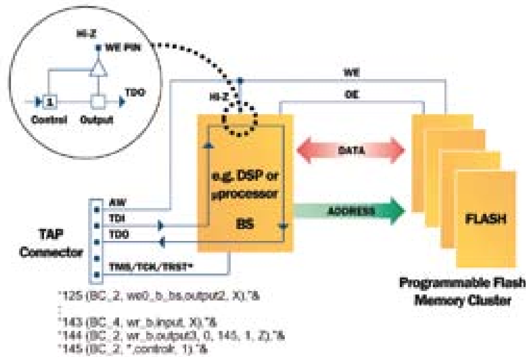

Figure. 9 - Eliminating Signal Contention

2.8.3 3-State and 2-State Output Cells

In the above example of the boundary register description the wr_b signal is described as a 3-state output cell in which the signal on this pin can be driven to logic “1”, logic “0” and also “high-z”. This is also depicted by the cell diagram at the top left of figure.8 in which a safe logic “1” value has been shifted into the cell 145 of the boundary scan register so that the output cell can be disabled. However, the we0_b_bs (cell 125) signal is described as a 2-state output cell in which the signal on this pin can only be driven to logic “1” or logic “0” and cannot be placed in high impedance. In this situation there will be contention between the we0_b_bs signal and the AWR signal.

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2.8.4 Multiple Output Cell Control

Alternatively the situation may prevail where each output cell does not have a unique control cell, and one control cell may control a number of output cells as shown in Figure.10.
In this example boundary scan cell 74 not only controls the WE signal but also controls other signals that are connected to the target flash memory device. Subsequently if a safe logic "1" value is shifted into cell 74, all signals associated with this cell will be placed in the high impedance state.

Figure. 10 - Multiple Output Cell Control

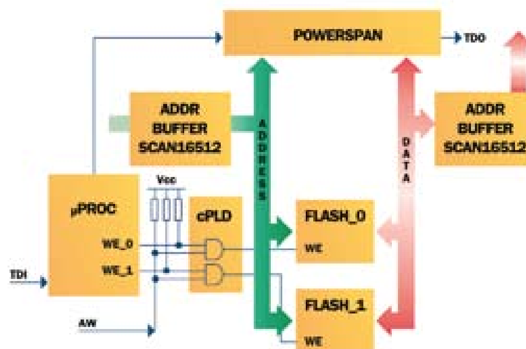
CHAIN_LIST

* CHAIN * POS	CELL NAME	PORT	FUNCTION	SAFE VALUE	[CCELL	DISABLE VALUE	RESULT]		
74	(BC_2 ,	*,	output2 ,	1			),	"	&
73	(BC_1 ,	WE,	output3 ,	0,	74,	1,	Z),	"	&
72	(BC_1 ,	OE,	output3 ,	0,	74,	1,	Z),	"	&
71	(BC_1 ,	nSDRAS,	output3 ,	0,	74,	1,	Z),	"	&
70	(BC_1 ,	nSDCAS,	output3 ,	0,	74,	1,	Z),	"	&
53	(BC_1 ,	A25,	output3 ,	0,	74,	1,	Z),	"	&
52	(BC_1 ,	A24,	output3 ,	0,	74,	1,	Z),	"	&
51	(BC_1 ,	A23,	output3 ,	0,	74,	1,	Z),	"	&
50	(BC_1 ,	A22,	output3 ,	0,	74,	1,	Z),	"	&

2.8.5 AutoWriteTM Gating Arrangement

With the scenarios depicted by figures 8 & 9, the only solution is to use some form of gating arrangement to select either the WE signal directly from the processor for mission mode operation. However for manufacturing test, the AW signal can be utilised to optimise the flash programming process. This gating arrangement can either be implemented using glue logic or could be embedded within a cPLD core. An example of this scenario is shown in Figure.11 below.

Figure. 11 - AutoWrite Gating Arrangement



2.8.6 Flash Programming Optimisation - Reducing Chain Length

The above example also shows how the flash programming process can be further optimised by significantly reducing the length of the boundary scan chain so that fewer bits are shifted for each flash memory read/write cycle. In the above scenario both the processor and the PowerSpan device have access to the target flash address and data lines, with the main control provided via the processor.

Subsequently the PowerSpan must be placed in high impedance, otherwise bus contention will prevail. If the PowerSpan device cannot be placed in the high impedance state by executing the HIGHZ instruction, the complete boundary scan register for the PowerSpan device will be added to the overall chain length, so that the safe values can be shifted into the relevant control cells to prevent the bus contention situation - this could equate to another 600 bits or more of data.

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2.8.7 Flash Programming Optimisation - Split Boundary-scan Data Register

Some custom asic designers have addressed the vector optimisation issue by designing the boundaryscan architecture so that the data register can be accessed as a split register Figure. 12.

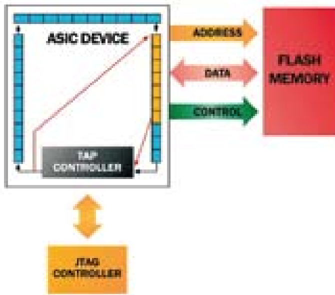

Figure. 12 - Split Boundary-scan Register

In this design the mandatory EXTEST instruction selects the complete boundary-scan data register comprising of 650 cells, whereas the device specific FLASH_PRG instruction selects the shorter (highlighted in yellow) data register comprising of only 125 cells. This type of configuration is extremely beneficial where the flash memory can be accessed via a custom device and the asic designer has the freedom to implement the device specific boundary-scan architecture to meet the board level DFT requirements.

2.8.8 Flash Programming Optimisation - Use of Boundary Scan Buffers

Alternatively this situation could be resolved by utilising 1149.1 compliant buffers, similar to the National Semiconductor SCAN16512 transceivers, which provide direct access to the target flash memory, data, address and control lines, including the WE signals. This would significantly reduce the chain length by only accessing the signals required to perform read/write accesses to the target flash memory, and not have the overhead of the many extra bits when only approximately 60 signal pins require to be accessed.

2.8.9 Flash Programming Optimisation - Embedded Flash Controller

Many alternative techniques for optimising the flash programming process are presented annually at Test Conferences throughout the world. Philips Research based in the Netherlands, presented a paper at the International Test Conference in 2001 that used the concept of embedding a flash memory controller function within a programmable device (either a cPLD or FPGA) in the form of VHDL code and provide access to this embedded controller through the 1149.1 Test Access Port Figure. 13.

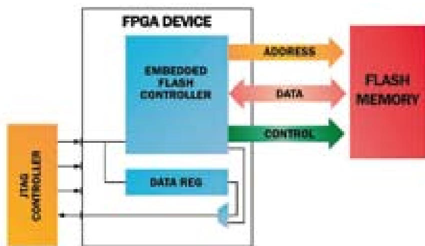

Figure. 13 - Embedded Flash Controller

The serial data path TDI/TDO provides access to the Data Register for loading the flash memory address and data values, whilst the embedded controller includes the programming algorithm for performing read and write access to an externally mapped flash memory device. Programming data is shifted into the embedded data register at the optimised TCK clock frequency, whilst other boundary-scan devices in the chain are placed in BYPASS or HIGHZ.

In this particular design implementation the pipelined Data Register can kept full at a TCK frequency of 8MHz, whilst read and write access to the flash memory is achieved at system clock speeds, achieving write cycles of typically 10us.

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2.9 Device Specific DFT Requirements

2.9.1 Dual Port Operation - Default Background Debug Mode (BDM)

Some boundary scan devices require special consideration in order to select the JTAG mode of operation. This is particularly the case where the boundary scan control pins have a dual multiplexed function and can be utilised for accessing the IEEE Std. 1149.1 TAP controller, or for accessing a proprietary debug port.

This becomes a problem where the default mode on power-up enables access to the proprietary debug port and not the 1149.1 TAP port. Under these circumstances it is not possible to gain access to the 1149.1 TAP controller in order to execute any form of boundary scan tests. An example of this power-up scenario is shown in Figure.14 below where the device will default to background debug mode unless specific data pins within the device Configuration Register are forced to the logic "1" and "0" state on power-up, at which point the 1149.1 TAP controller port will be selected.

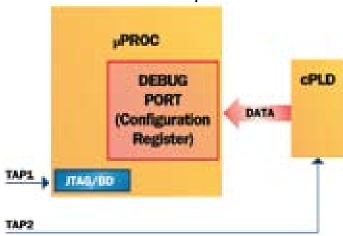

Figure. 14 - Forcing JTAG Operation on Power-up

2.9.2 Forcing JTAG Operation on Power-up

The control logic for establishing the correct configuration register status on power-up can either be implemented using glue logic or could be embedded within the core function of a cPLD, as shown in Figure.11 above.

However, if this function is embedded within a cPLD, that cPLD must be placed in separate boundary scan chain because the cPLD will have to be programmed with the core function and placed in BYPASS mode, so that after re-cycling power the processor will sense the correct configuration status.

If the cPLD was in the same chain as the processor, it would not be possible to program the cPLD with the control logic to force the processor into JTAG mode. Subsequently the chain would be effectively broken due to the default power-up status being the background debug mode of operation.

Note:- This type of problem exists on very few devices; however, it is imperative that you fully read the documentation for any boundary scan device that is being implemented within board designs, to ensure that there are no hidden pitfalls that need considering before devices function in boundary scan mode.

2.10 Design-for-Test - Other Considerations

2.10.1 Control of Watchdog Circuits

Under certain test conditions it is recommended that any on-board watchdog circuit can be disabled throughout the duration of boundary-scan testing. Otherwise the watchdog circuit may reset the onboard processor, which will place this device in Test-Logic-Reset (TLR) causing the device to return to its normal operational mode and subsequently breaking the boundary-scan chain. This situation is most likely to happen during a prolonged test sequence which will exceed the watchdog timeout period i.e. flash programming.

If possible control the watchdog disable circuit via an unused boundary-scan cell or by placing a jumper in the prescribed position on a test header.

2.10.2 Configurable Termination Resistors

It is advisable not to rely on the use of configurable pull-up/pull-down resistive termination within FPGA devices to control logic within a board design because these programmable terminations will not be active whilst the device is in the pre-configured state. This may lead to unreliable operation during test.

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3 Contact Information

For more information of JTAG Technologies:
If you want to apply boundary-scan for testing or in-system programming and you need more help or you need product information, please contact:

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For contacting JTAG Technologies' local sales representatives, see our website at www.jtag.com/sales.

IEEE Standards:
- IEEE Std 1149.1-2001 - IEEE Standard Test Access Port and Boundary-Scan Architecture (Supersedes former issues IEEE 1149.1-1990 (Including 1149.1a-1993) and IEEE 1149.1b-1994 and errata)
- IEEE Std 1532-2001 - IEEE Standard for In-System Configuration of Programmable Devices (Supersedes IEEE 1532-2000)

For more information on the IEEE Standards:
IEEE Customer Service
445 Hoes Lane, PO Box 1331
Piscataway NJ 08855-1331 USA
T: (800) 701 4333 (within the US and Canada)
T: (732) 981 0060 (outside the US and Canada)
F: (732) 981 9667
E: customer.service@ieee.org
W: www.ieee.org

For more information on JEDEC:
If your company designs its own ASICs with boundary-scan and you want to get a JEDEC Manufacturer ID Codes (JEP106), please contact JEDEC - Technical Affairs of the Electronic Industries Alliance (EIA) at:
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F: +1 703 907 7583
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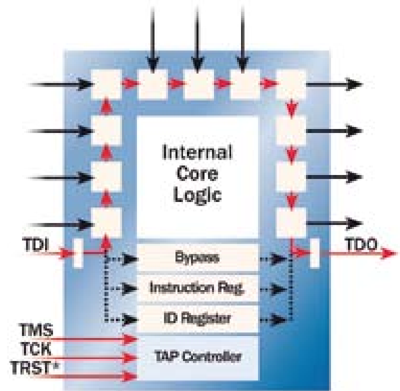
4 Principle of boundary-scan

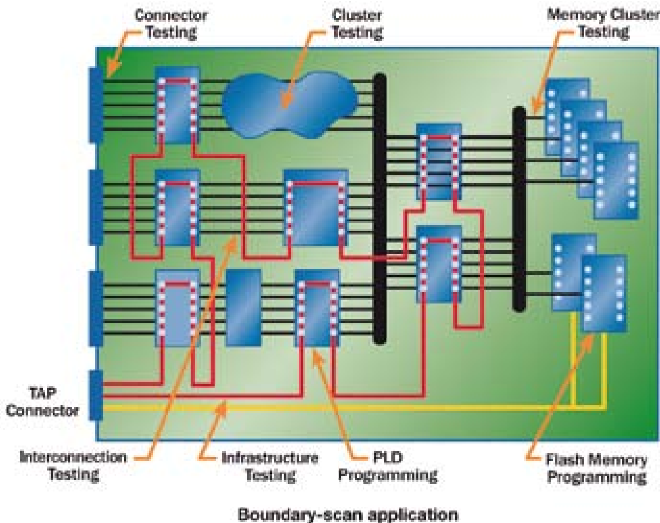
The principle of boundary-scan

The IEEE 1149.1 standard defines a four-wire serial interface (a fifth wire is optional) to access complex integrated circuits (ICs) such as microprocessors, DSPs, ASICs, and CPLDs. Most of today's complex ICs are already supporting this feature. Any compatible IC contains shift registers and a state machine to execute the boundary-scan functions. Data enters serially the chip on the TDI pin and leaves the chip on the TDO pin. The boundary-scan logic is clocked by the TCK signal, independent of the system clock. The TMS signal controls the state machine and TRST* is optional for a hardware reset signal.



IEEE 1149.1 Device Architecture

Multiple scan-compatible ICs may be serially interconnected on the printed circuit board, forming the boundary-scan chain, and a board may contain more than one scan chain. The scan chain provides electrical access, from the serial TAP interface, to every pin on every IC that is part of the chain. In normal operation, a scan-compatible IC performs its intended function as though the boundary-scan circuits were not present. However, when testing or in-system programming is to be performed, the device's scan logic is activated. Data can then be sent to the IC and read from it using the serial interface.
This data may be used to stimulate the device core, drive signals outward to the PCB, sense the input pins from the PCB, or sense the device outputs. The scan modes of operation provide the ability to test a board for manufacturing structural faults and to perform in-system device programming all via the standard JTAG TAP.



Boundary-scan application

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4 Glossary of Abbreviations:

ASIC Application Specific Integrated Circuit
AW AutoWrite
BDM Background Debug Mode
BGA Ball-Grid Array
BSDL Boundary-Scan Description Language
BSR Boundary-Scan Register
cPLD Complex Programmable Logic Device
DFT Design for Test(ability)
DIOS Digital Input Output Scan
DNP Do Not Place
DSP Digital Signal Processor
ECL Emitter Coupled Logic
FPGA Field Programmable Gate Array
Hi-Z High Impedance
I/O Input - Output
IC Integrated Circuit
ICT In-Circuit Test(ing)
IEEE Institute of Electrical and Electronic Engineers
IP Intellectual Property
IR Instruction Register
ISP In-System Programming
JEDEC Joint Electron Device Engineering Council
JTAG Joint Test Action Group
LSP Local Scan Port
LVTTL Low Voltage Transistor - Transistor Logic
MCGR Multi-Cast Group Register
OE Output Enable
PCB Printed Circuit Board
PLL Phase Locked Loop
SDRAM Synchronous Dynamic Random Access Memory
SI Scan Input
SO Scan Output
SRAM Static Random Access Memory
SSRAM Synchronous Static Random Access Memory
TAP Test Access Port
TCK Test Clock
TDI Test Data Input
TDO Test Data Output
TMS Test Mode Select
TRST Test Reset
TTL Transistor - Transistor Logic
UUT Unit Under Test
VLSI Very Large Scale Integration
WE Write Enable

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